

FIG. 2a

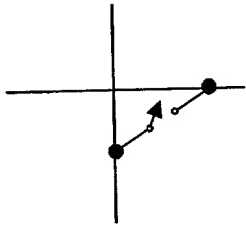


FIG. 2b

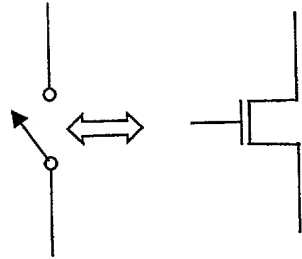


FIG. 2c

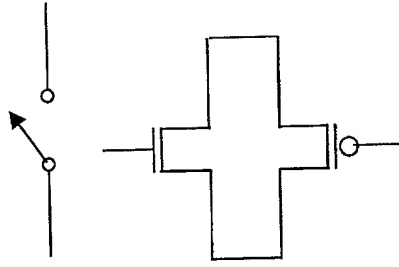


FIG. 2d

FIG. 2 (Prior Art)

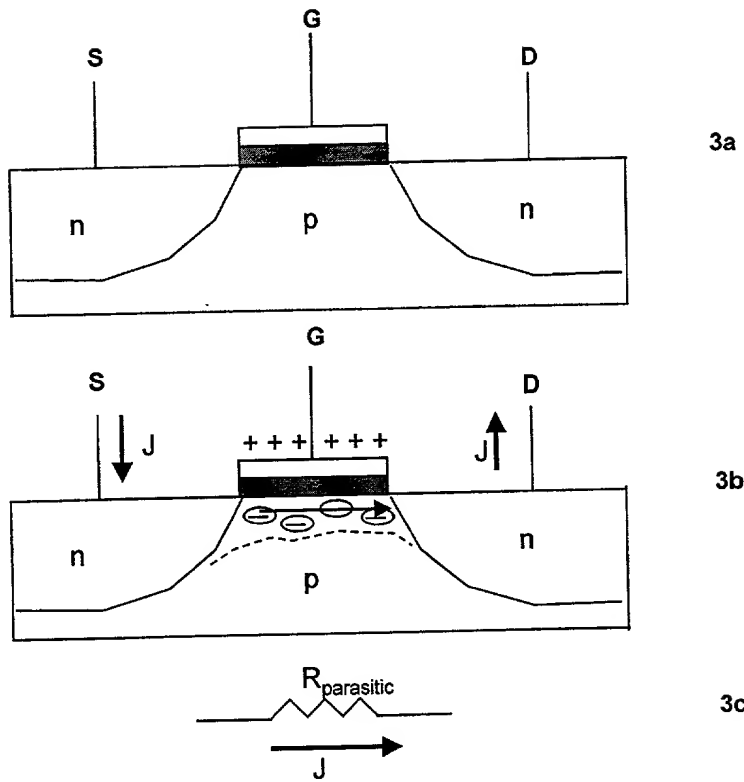


FIG. 3 (Prior Art)

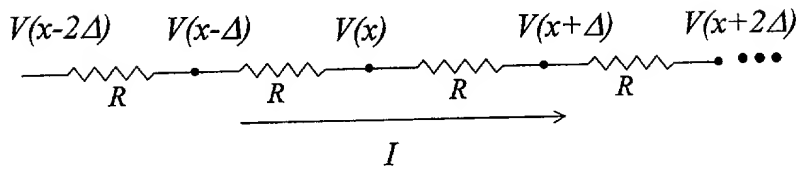


FIG. 4

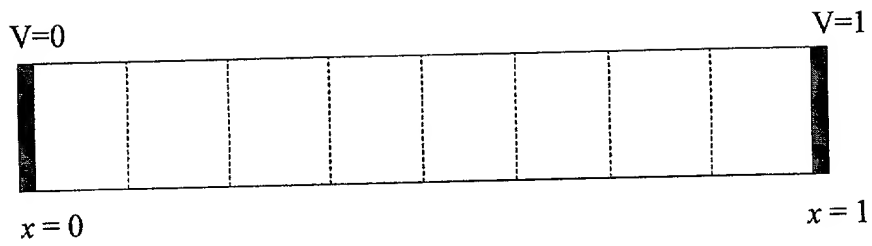


FIG. 5a

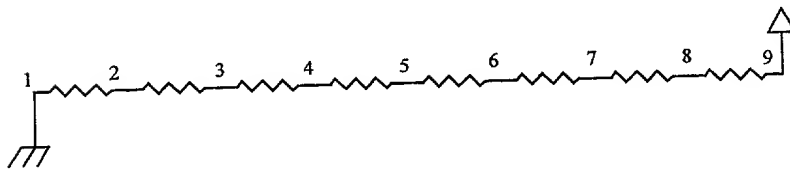


FIG. 5b

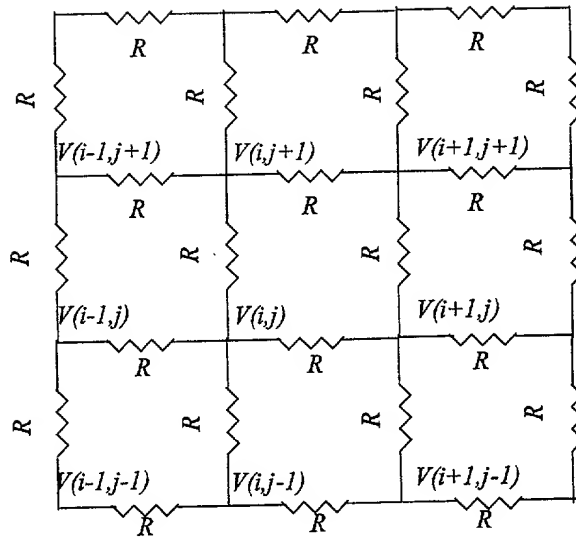


FIG. 6a

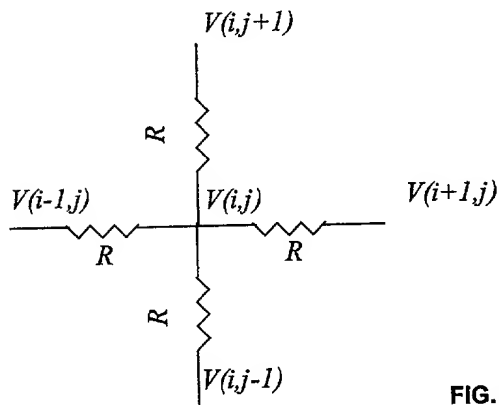


FIG. 6b

FIG. 7a

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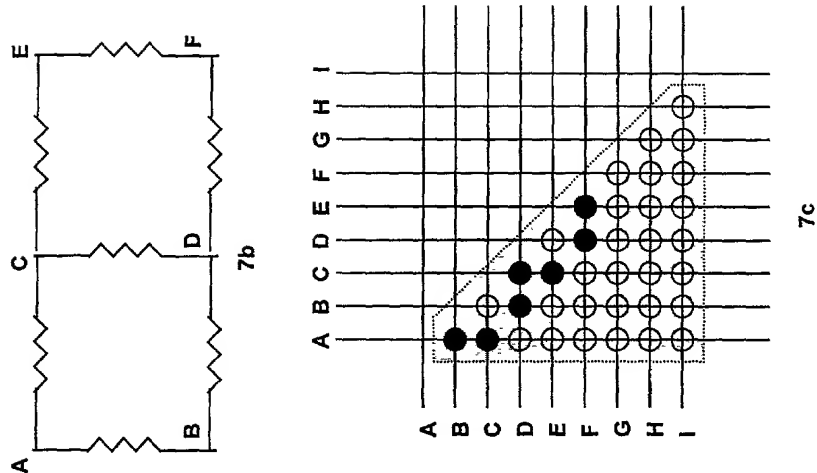
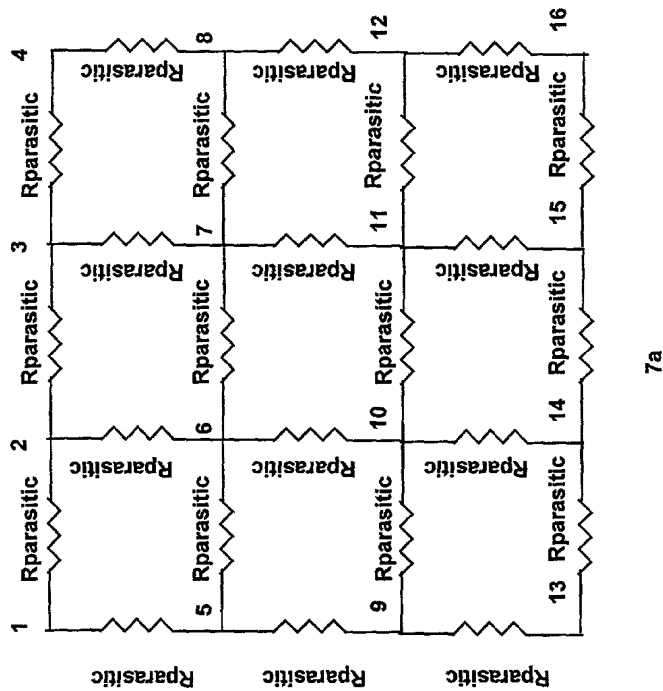


FIG. 7

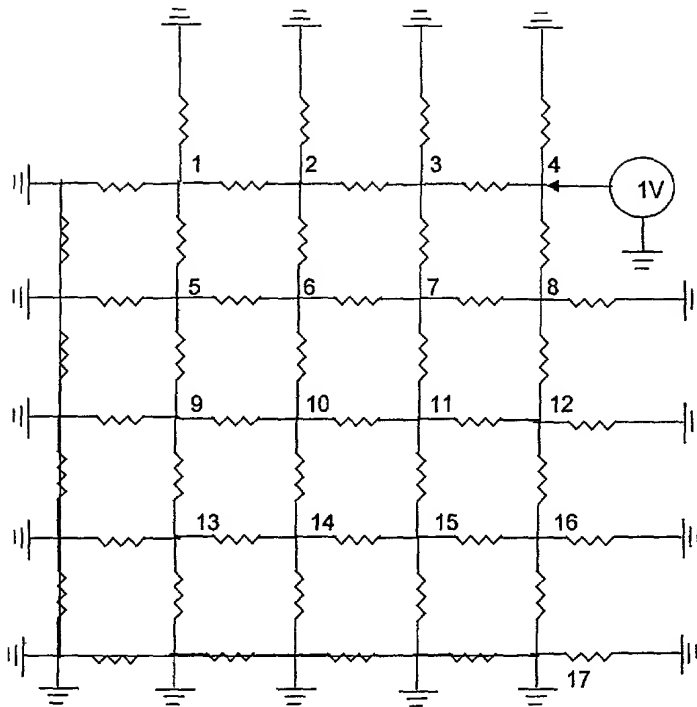


FIG. 8a

Pin	Close switches within FPID as required to connect to pin
1	2,5,17
2	6,3,17 (connection to pin 1 is already achieved)
3	4,7,17
4	8,17
5	6,9,17
6	7,10
7	8,11
8	12,17
9	10,13,17
10	11,14
11	12,15
12	16,17
13	14,17
14	15,17
15	16,17
16	17

FIG. 8b

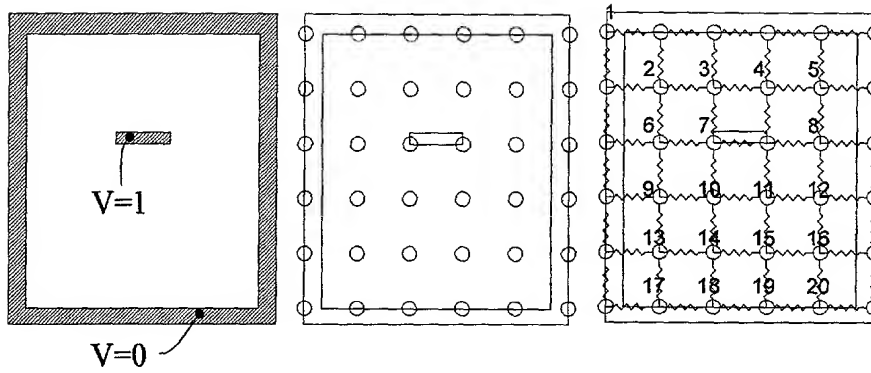


FIG. 9a

Pin #	Voltage
1	0
2	0.187919
3	0.395973
4	0.395973
5	0.187919
6	0.355705
7	1
8	0.355705
9	0.234899
10	0.47651
11	0.47651
12	0.234899
13	0.107383
14	0.194631
15	0.194631
16	0.107383

FIG. 9b



APPROVED FOR RELEASE BY NSA ON 08-28-2013 pursuant to E.O. 13526, 2013-08-28

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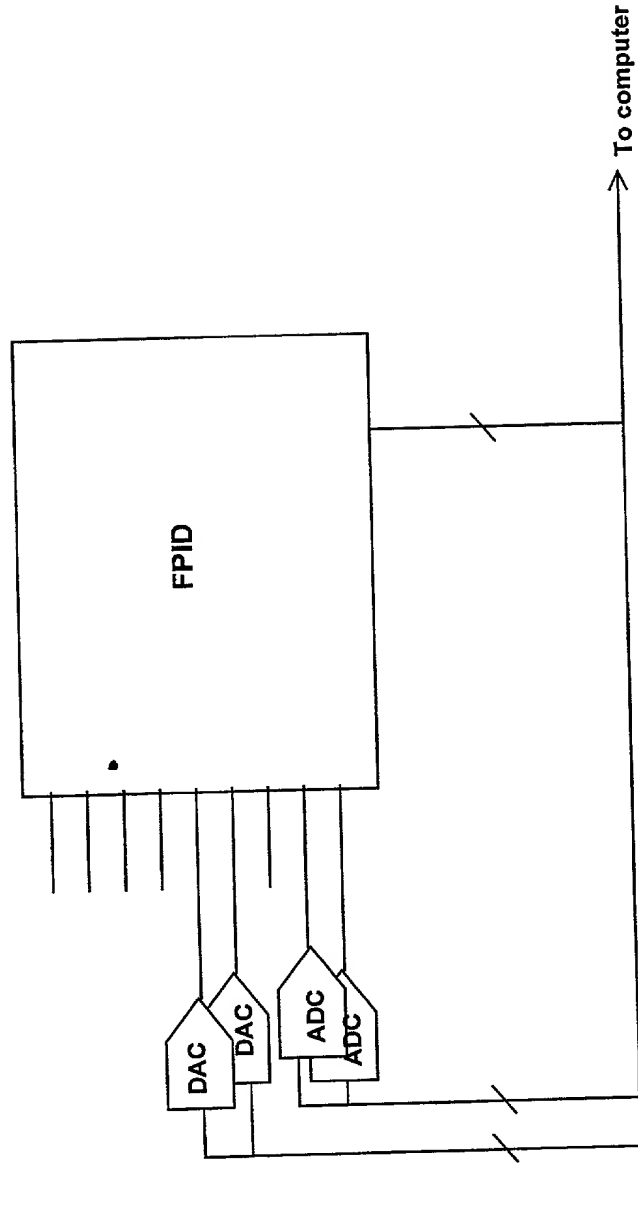


FIG. 10



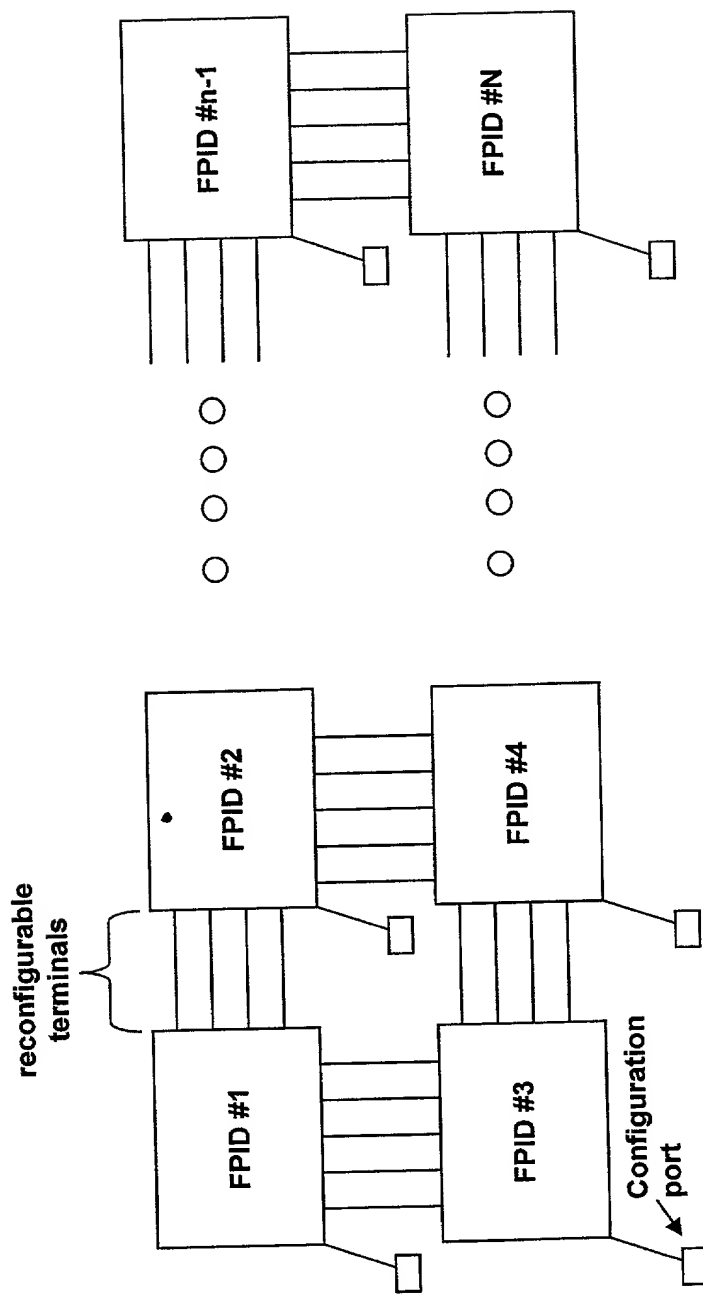


FIG. 12

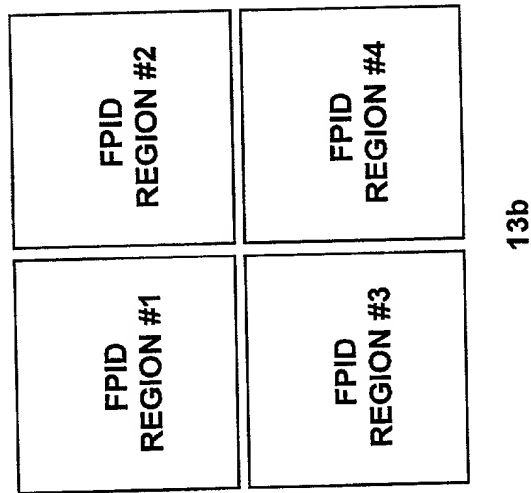
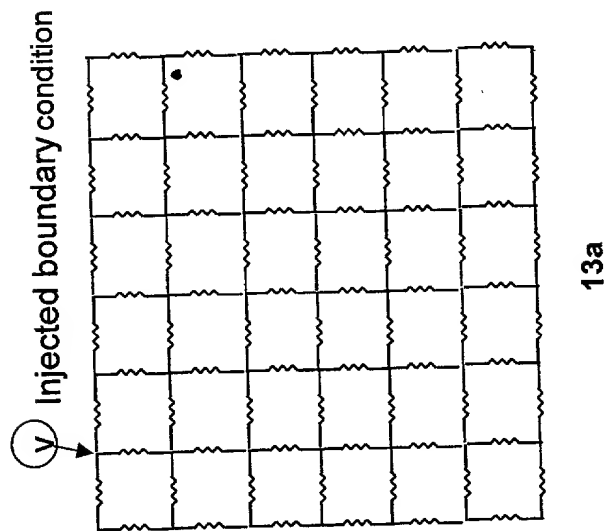


FIG. 13

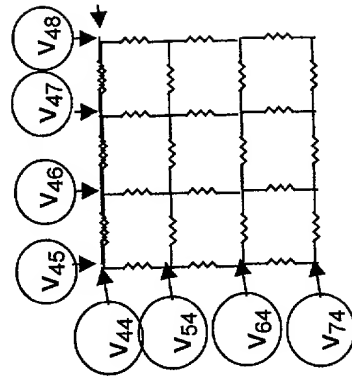
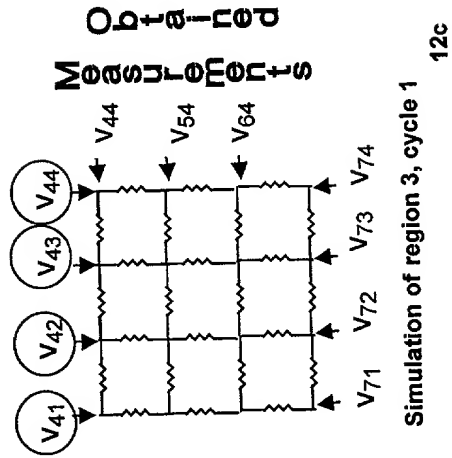
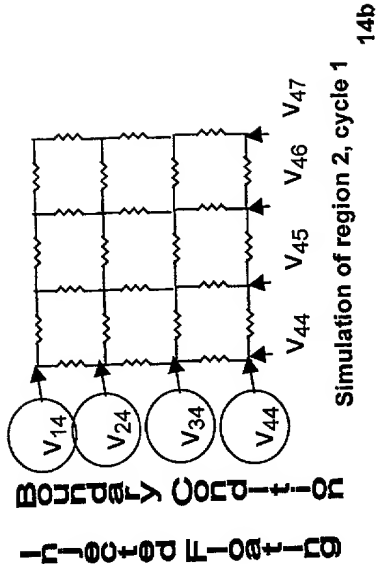
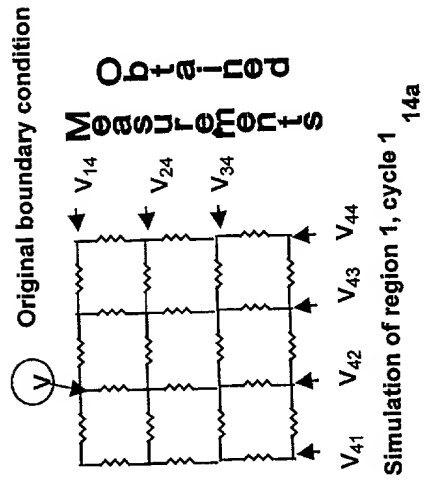


FIG. 14